Digital and Mixed Signal Testing Technology the Standards IEEE 1149.1 and IEEE 1149.4

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Abstract- *Among all the On-Chip built-in self-test (BIST) technologies, JTAG is the most well-known and widely used. In this paper, the mechanism of basic JTAG (IEEE 1149.1) has been discussed. The pitfalls of the method are also discussed, some of which are rectified in the future standard, IEEE 1149.4 for Mixed Signal testing, which is also described here. Many of the valuable research papers on these standards are analyzed.*

Keywords*- IEEE 1149.1, IEEE 1149.4, JTAG, Boundary Scan, BSDL, Mixed Signal, SoC.*

I. INTRODUCTION

Starting from mid ’70s, the structural testing of the PCB circuits has been done using the traditional in-circuit mechanism which is often known as bed-of-nails technique. This method uses several pins inserted into holes in an acrylic plate which are associated to make contact with test points on a PCB and are also connected to a measuring unit by wires. In this technique, a physical access to all the components on the PCB is must. For the modern circuits and chips, which use thousands of components connected with a multi-layer PCB, especially for BGA circuits, the physical contact is almost impossible. In such a situation, a group of test engineers coming from some European electronics company jointly formed a group called Joint European Test Action Group (JETAG). They proposed a novel solution which is known as JTAG later. The technique was based on the use of shift register placed around the boundary of the chip, that’s why popularly known as “boundary scan” method. In this paper, Section II describes the principle used behind the standard IEEE 1149.1. Section III analyzes the pit-falls of IEEE 1149.1, the motivation behind the development of IEEE 1149.4 and the principle used for IEEE 1149.4 for mixed signal testing. In the Section IV, a comparative study is given on the important papers on these mostly used technologies. Section V summarizes the works yet to be done.

II. THE PRINCIPLE OF BOUNDARY-SCAN USED IN IEEE 1149.1 (JTAG)

The heart of the Boundary- Scan architecture is the series of boundary cells/modules (registers) placed along the periphery of the device. The cells connected with the device’s primary inputs and with primary outputs are called as input cells and output cells respectively. The scan cells are basically the shift registers connected in a parallel-in, parallel-out fashion. At the time of loading, also called capturing, the signal values from the input pins are loaded in a parallel way into the input cells and the signal values from the core logic are copied into output cells. The unload operation; also called update operation is also a parallel operation where the signal values are passed from output boundary cells to the output pins. Data can be entered into the Test Data in (TDI) which move through the shift register in serial mode and can be captured from the output pin Test Data Out (TDO). The test clock pin is referred as TCK. TMS is the serial control signal which controls the mode of operation. These four pins are collectively called Test Access Port (TAP).

III. IEEE 1149.4 FOR MIXED SIGNAL TESTING

We have briefly discussed the most widely used technology IEEE 1149.1 (JTAG) above, but the success of JTAG is limited within the digital chip testing domain. The trend of making ICs with analog, digital, and mixed-signal circuits on the same substrate is increasing day by day. Designers prefer to integrate analog and digital devices on the same chip for reducing circuit packaging and assembly costs. Now-a-days, more than 50% of IC and boards are of mixed signal types. So by using IEEE 1149.1, the analog pins cannot be handled by the testing technology itself. At the same time, the passive analog components are getting too small to probe externally.

For testing of Mixed Signal cores, a technique is developed known as IEEE 1149.4 [1, 3, 4, 26] which is basically the extension of IEEE 1149.1. In this technique, both the analog and digital parts can be tested through the IEEE 1149.4 port. To use this strategy, all the SoC chips have to have both the analog and digital test pins which connect the chips with the external world. The mixed signal testing technique using IEEE 1149.4 is beneficial in terms of testing cost and time-to-market.

IEEE 1149.4 includes some extra components than IEEE 1149.1 to incorporate the analog testing mechanism along with the digital testing. Like the digital test modules, there are some analog boundary modules (ABM), which are placed between the core circuit and analog function pins to give and collect analog test data. Analog pins are the pins connected from externally that are intended to pass information. The test data can be current or voltage having value

within a certain range defined by the driver or receiver used for testing. Analog pins can also pass digital data which falls within their range.

Like Test Access Port (TAP) used in JTAG, Analog Test Access Port (ATAP) is used in IEEE 1149.4 which consists of two mandatory and two optional pins. The mandatory pins are AT1 and AT2. The pins are attached with an analog bus. The analog test equipment can be connected with the pins to access the SoC's internal analog test facilities. Differential testing can also be done using the optional pins.

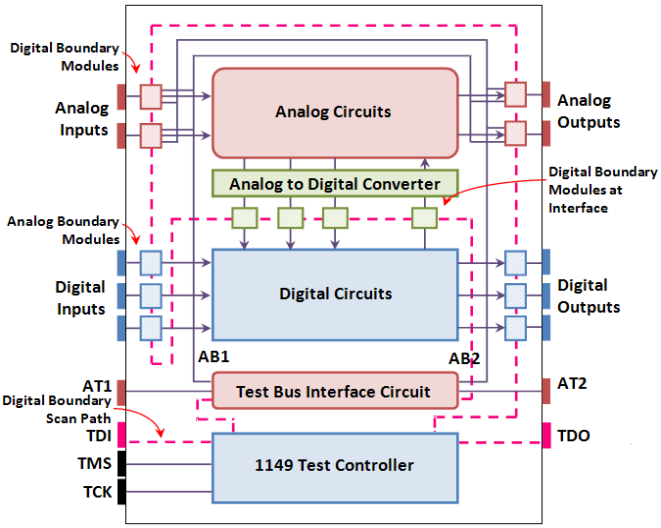

Figure 1. IEEE 1149.4 for Mixed-Signal testing

IEEE 1149.4 is mainly intended for 3 kinds of testing for SoC i.e. Interconnect test which checks the open and short connections, Parametric test which measures the analog characteristics of the components and Internal test to perform ample tests on the components which may be either in isolation or mounted on a substrate.

IV. STUDY ON IEEE 1149.1 AND 1149.4

As the scope of physical access to the components is decreased, various testing methods are required to detect the faults in the structural testing, as the fault detection using functional testing increases cost. The same chip level boundary-scan algorithm can be used for digital circuit card assemblies as well as for system level testing. In case of any firmware update or stress screening with pin-level diagnosis upon failure, system-level boundary-scan enables a fast and inexpensive method to perform the task without disassembling it. Also before sending the product to market, system testing can also be done using boundary-scan technique. In case of POST, the same boundary-scan technique can also be used by an embedded boundary-scan controller to perform embedded boundary-scan test. The Built-In Test (BIT) of a chip/board can be initiated remotely through the target's serial communication channel or other I/O ports for remote test and diagnostics [25].

In today's world, most of the PCBs contain a large number of analog clusters. There is a number of publications who have addressed test-land minimization for the Mixed signal PCBs and boards.

The on-chip Mixed-Signal Design for Testability (DFT) and the IEEE 1149.4 testing methods can be reused to reduce the number of test pins required for those boards [2, 3]. Being a BIT method, it gives better diagnostic resolution than a functional test of the system. Though, using 1149.4, multiple regions cannot be tested simultaneously, but better signal quality and bandwidth can be achieved which can help to detect more errors using high quality equipment. The on-chip Mixed-Signal DFT method has the advantage that there is no need of external measurement equipment or additional on-chip DFT for board test. They can easily and quickly generate tests for analogue clusters. At the time of design phase this method can be widely used as testing is very much essential parallel to the design changes, which reduces Time-To-Market. When actual production is started, the method helps to reduce the number of test pins. One of the good BIST method is proposed in [6] called VDDQ, which takes less area to implement. In this method, the quiescent voltage of the nodes of CUT are sensed serially and compared with their normal value. The result is a 10 bit digital vector, containing a pass-fail flag and the analog voltage sensed.

Now-a-days, all electronic products have to pass through a functional test before they are deployed to market. Functional Tests, though a mandatory part of manufacturing electronic products, however, require manual testing using ad-hoc test equipment configurations. The process is a labor intensive and requires test plan and data coming from some costly test development process. So it will be beneficial if Boundary Scan technique can be combined with Functional Test which is presented in the recent paper [7] termed as Extended Boundary Scan technique based on reconfigurable tester hardware.

JTAG architecture requires 5 external connections between JTAG controller and target IC's JTAG port, which increases the pin-out resulting the increase in chip area. The paper [8] proposed an excellent solution for this problem. Here a Parallel-to-Serial interface was used to serialize the data coming from the five pins and pass through 1 or 2 lines. Serial-to-Parallel interface placed inside the target IC transformed the serial data into parallel for the 5 JTAG pins. The use of Simultaneously Bi-directional Transceiver (SBT) technology made possible to increase the serial communication speed using high speed Full Duplex communication through a single wire [9-12]. This technology can be applied in IEEE 1149.4 also. The paper [13] proposed a method to perform boundary scan and full scan through a common IEEE 1149.1 interface to reduce the pin count.

The Boundary Scan Description Language (BSDL) has been designed as the standard

programming language for boundary scan devices following IEEE 1149.1 standard, which enables users to provide a description of the way in which boundary scan applies to different devices. In the paper [14], a language was presented that can describe the boundary-scan algorithm for a mixed-signal device (ABSDL). It is almost a complete language which is basically the extension of BSDL that uses VHDL to define the required components which supports both of the key features of IEEE 1149.4, the Test Bus Interface Circuit (TBIC) and Analog Boundary Module (ABM).

A numbers of software tools and CAD tools are developed to generate test vectors to detect the faults in mixed-signal boards. Circuit Analyzer and Test Generator (CATGEN) [3] are two of them which operate on their schematic information. The pseudo-code generated by CATGEN can automatically be translated into functional tests by Automated Control Program (ACEPro).

Several research works are done to implement DFT in the analog testing domain. Two such methods are presented in [15] and [16]. In the paper [18], a CAD tool was presented using Analog and Mixed-Signal DFT (AMSDFT).

One of the drawbacks of IEEE 1149.4 is that it is only targeted for the low frequency testing as it is basically the extension of JTAG boundary scan. This creates a major challenge for measuring the new RF standards such as Bluetooth and IEEE 802.11 (Wi-Fi). In [20], an under-sampling method was reported where a CMOS transmission gate was used driven by a repetitive, narrow sampling pulse. In this paper, constant-width pulses of 0.5 to 2 ns duration were applied at 1 MHz sampling frequency while input frequency was above 100 MHz. A sampling gate was used connected to an on-chip bus that acted like a 1 pF hold capacitance. The bus was connected with a low-speed unity-gain buffer connected to an output pin.

A similar kind of under-sampling method is described in [19]. In the traditional under-sampling technique, a sample-and-hold circuit was used to capture the HF signal value at some particular instances. The article described the technique used in sampling oscilloscope to show the full amplitude HF signals. Sample-and-hold technique requires a sampling switch, an on-chip capacitor and a high speed op-amp or buffer when used along with IEEE 1149.4. The experimental results were shown in the paper [21]

The paper [18] proposes an excellent technique to use IEEE 1149.4 in such a situation. They actually proposed a RF-to-LF circuitry which actually sub-samples the RF signal, i.e. samples with a rate less than the frequency of the signal. A narrow-band RF signal can easily sub-sampled using the Fourier distribution as the narrow-band RF signal can be produced around the multiples of the sampling frequency. The desired harmonic can easily be extracted with the help of a low-pass filter.

Another excellent ABM method was presented in [22] compatible with IEEE 1149.4. Here information are extracted from the RF signal and are converted into corresponding DC voltage level. This paper demonstrated when the frequency range is set between 1 GHz to 2 GHz, it gives an error of roughly 2 dB in measuring the power, caused by temperature, supply voltage and process variations, along with a 0.1 GHz error in the frequency measurement.

The IEEE 1149.4 technology can be implemented in the environments where automotive systems take the major part; most of them are the part of safety critical applications. The paper [23] presented an application of IEEE 1149.4 and the Integrated Diagnostic Reconfiguration (IDR) in an Automotive Electronic Control Unit developed using a fully integrated mixed signal system. Fault Avoidance can be implemented in a Mixed-Signal system which can handle the key failures.

V. Conclusion and Future Scope

This paper reports the current works in the IEEE 1149.1 and IEEE 1149.4 field, which are obviously the first choice of the chip test engineers using Boundary Scan technique. Due to space limitation, all the works cannot be documented here, covering the major fields in those standards, especially the IEEE 1149.4.

IEEE 1149.4, the famous technique for Mix-Signal testing requires the pin-outs for all the analog and digital test pins, which actually increases the pin-count and chip area as well as the power requirement. The paper [24] proposed an excellent technique to minimize the pin-outs by producing the analog test-signals from the digital test inputs using a DAC, assuming the analog part is embedded within the digital part. But in a usual SoC, the analog part which contains fewer components with respect to the digital components actually interconnects the digital core with the external world. So, when the digital blocks are embedded within the analog block, then it is not possible to give the test vectors directly to the inputs of the digital block. Now if the analog block itself can be used to give the inputs for the embedded digital block, then the count of test pin-out can be minimized, minimizing the chip area and cost. This may be a good topic for the future researchers. Table 1 provides a comparative study among the works done so far on Digital, Analog and Mixed-Signal testing.

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TABLE I. COMPARATIVE STUDY

Papers	VDDQ with the output of 10 bit digital vector	Boundary Scan combined with Functional Testing	**Analog BSDL**	Analog Boundary Scan Description Language	**Analog DFT**	System Level Testing for large analog system	**CAD Tools**	CAD based on Schematic Information	CAD based on Analog DFT	**Radio Frequency Sampling**	RF-to-LF Using Fourier Analysis	RF-to-LF Using Sampling Oscilloscope technique	Board Level Testing with frequency > 10 MHz	Using CMOS Transmission Gate	Low Error in Freq and Power measurement in 1 to 2 GHz	**Chip Area Reduction**	Serialize 5 JTAG pins into one or two	Combination of DFT, boundary-scan and full-scan	Construction of Analog test-inputs using Digital ones
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