

# Improved Design of Low Power TPG using LP-LFSR

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**Abstract**— This paper presents a novel test pattern generator which is more suitable for built in self test (BIST) structures used for testing of VLSI circuits. The purpose of the BIST is to reduce power dissipation without affecting the fault coverage. The demonstrated test pattern generator reduces the switching activity among the test patterns at the most. In this method, the single input change patterns generated by a counter and a gray code generator are Exclusive-ORed with the seed generated by the low power linear feedback shift register [LP-LFSR]. The proposed scheme is evaluated by using a 4x4 Braun array multiplier. The System-On-Chip (SOC) approach is adopted for implementation on Altera Field Programmable Gate Arrays (FPGAs) based SOC kits with Nios II soft-core processor. From the implementation results, it is verified that the testing power for the proposed method is reduced by a significant percentage.

**Keywords**— FPGA, BIST, LP-LFSR, Switching activity

## I. INTRODUCTION

In VLSI circuits, built in self test (BIST) are used for testing. The objective of the BIST is to reduce power dissipation without affecting the fault coverage[1]. The main challenging areas in VLSI circuits are cost, performance, reliability, power, testing and area. The demand for portable computing devices and communication system are rapidly increasing. These applications require low power dissipation for VLSI circuits[2]. The ability to design, fabricate and test Application Specific Integrated Circuits (ASICs) as well as FPGAs with gate count of the order of a few tens of millions has led to the development of complex embedded SOC. Hardware components in a SOC may include one or more processors, memories and dedicated components for accelerating critical tasks and interfaces to various peripherals. One of the approaches for SOC design is the platform based approach. For example, the platform FPGAs such as Xilinx Virtex II Pro and Altera Excalibur include custom designed fixed programmable processor cores together with millions of gates of reconfigurable logic devices.

In addition to this, the development of Intellectual Property (IP) cores for the FPGA's for a variety of standard functions including processor's, enables a multimillion gate FPGA to be configured to contain all the hard-core processors and they can be enhanced with custom hardware to optimize them for specific application. Power dissipation is a

challenging problem for today's System-on-Chips (SOCs) design and test.

The paper is organized as follows. In section II, literature survey relevant to power reduction are explained, which mainly concentrated to reduce the average and peak power. In section III, an overview of power analysis for testing is presented. The section IV, explains a simple braun array multiplier, which is taken here as a circuit under test (CUT) to verify the effectiveness of the proposed technique. In Section V, the proposed technique in the test pattern generator is described. Section VI explains the algorithm for the proposed LP-LFSR. In section VII, implementation details are explained.

## II. LITERATURE SURVEY

Y.Zorian[3] presented that the power dissipation of a system in test mode is more than in normal mode. P.Girard[4] demonstrated that four reasons are blamed for power increase during test.

- Due to nature of test patterns, high switching activity occurs.
- During test mode, parallel activation of internal cores happens.
- Extra design-for-test (DFT) circuitry consumes power.
- Low correlation among test vectors.

Mechrdad Nourani[5] explained that this extra average power consumption and peak power consumption can create problems such as instantaneous power surge that cause formation of hot spots, circuit damage, difficulty in performance verification and reduction of the product field and life time. Thus, special care must be taken to ensure that the power rating of circuits is not exceeded during test application. Different types of methods are stated to control the power consumption. These methods mainly includes algorithms for test scheduling with minimum power, techniques to reduce peak power and average power, techniques for reducing power during scan testing and BIST(built-in-self-test) technique. In order to minimize the time required for adjustment of the parameters, off-chip communication between a processor and the FPGA is bound to be slower than on-chip communication.

The BIST (built-in-self-test) approach using design for testability technique is presented for this case.

Different techniques are available to reduce the switching activities of test pattern, which reduces the power in test mode. P. Giard [6] proposed a modified clock scheme for linear feedback shift register (LFSR), in which only half of the D flip-flops works. Thus, only half of the test pattern can be switched. S.K.Guptha [7] determined a BIST TPG for low switching activity in which there is d-times clock frequency between slow LFSR and normal LFSR and thus, the test pattern generated by original LFSR is re-arranged to reduce the switch frequency. Mehrdad Nourani [5] presented low transition test pattern generator (LT-TPG) which reduces the average and peak power of a circuit during test. The above said techniques can reduce the average power compared to traditional linear feedback shift register (LFSR).

A better low power can be achieved by using single input change pattern generators. I.Voyiatzis et al., [8] and S.C.Lei et al., [9] demonstrated that the combination of scan shift register and LFSR are used to generate random single input change sequences. S.C.Lei et al., [9] and R.H.He et al., [10] proposed that (2m-1) single input change test vectors can be inserted between two adjustment vectors generated by LFSR where m is length of LFSR. BOYE and Tian-Wang Li [11] proposed that  $2^m$  single input changing data is inserted between two neighbouring seeds. The average and peak power are reduced by using the above techniques. Still, the switching activities will be large when clock frequency is high.

### III. POWER ANALYSIS FOR TESTING

In CMOS technology, the power dissipation can be classified into static and dynamic. Static power dissipation is mainly due to the leakage current. Dynamic power dissipation is due to switching transient current and charging and discharging of load capacitances. Some significant parameters for evaluating the power consumption of CMOS circuits are discussed below.

$$E_i = \frac{1}{2} C_0 V_{dd}^2 CFS \quad (1)$$

Where  $V_{dd}$  is the supply voltage,  $C_0$  is the load capacitance. The product of  $F_i$  and  $S_i$  is called weighted switching activity of internal circuit node  $i$ .

The average power consumption of internal circuit node  $i$  can be given by,

$$P_i = \frac{1}{2} C_0 V_{dd}^2 CFS f \quad (2)$$

$f$  is the clock frequency. The summary of  $P_i$  of all the nodes is named as average power consumption. It can be observed from (1) and (2) that the energy and power consumption mainly depends on the supply voltage, switching activities and clock frequency. This paper reduces the switching activity as low as possible at the inputs of the circuit which is under test.

#### A. BIST Approach:

BIST is a design for testability (DFT) technique in which testing is carried out using built-in hardware features. Since testing is built into the hardware, it is faster and efficient. The BIST architecture shown in fig.1 needs three additional hardware blocks such as a test controller, a test pattern generator and output response analyzer.

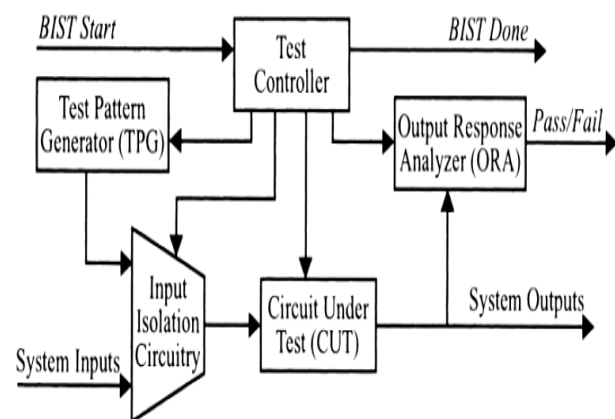


Fig.1 BIST basic block diagram

A test controller provides a control signal to activate all the blocks. For test pattern generators, we can use either a ROM with stored patterns, or a counter or a linear feedback shift register (LFSR). A response analyzer is a compactor with stored responses or an LFSR used as a signature analyzer.

BIST has some major drawbacks where architecture is based on the linear feedback shift register [LFSR]. The circuit introduces more switching activities in the circuit under test (CUT) during operation test than that during normal operation. R.S.Katti et al., [12] proposed that it causes excessive power dissipation and results in delay penalty into the design.

### IV. DESIGN OF MULTIPLIER

In DSP operations, multipliers are widely used such as convolution for filtering, correlation and filter banks for multi-rate signal processing. Without multipliers, no computations can be done in DSP applications. For that reason, multipliers are chosen for testing in our proposed design. Braun array multiplier is selected among various multipliers as

it follows simple conventional method as shown in figure2.

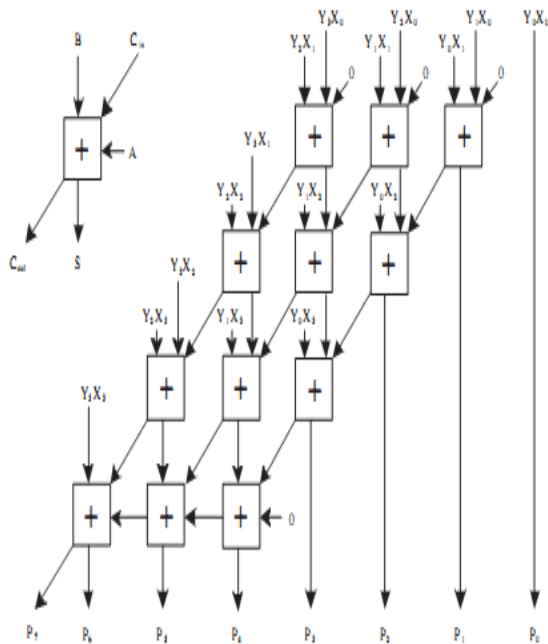


Fig.2 Braun array multiplier

V. PROPOSED METHOD

Linear feedback shift register [LFSR] is used due to the simplicity of the circuit and less area occupation, for generating test patterns. In this paper, we determined a novel architecture which generates the test patterns with reduced switching activities. Figure3 shows the Low power test pattern generator (LP-TPG) structure consists of modified low power linear feedback shift register (LP-LFSR), m-bit counter, gray code generator, NOR-gate structure and XOR-array.

The m-bit counter is initialized with Zeros and which generates  $2^m$  test patterns in sequence. A gray code generator and m-bit counter are controlled by common clock signal [CLK]. The output of m-bit counter is applied as input to a NOR-gate structure and a gray code generator. When all the bits of counter output are Zero, the NOR-gate output is one. Only when the NOR-gate output is one, the clock signal is applied to activate the LP-LFSR which generates the next sequence. The sequence generated from LP-LFSR is Exclusive-ORED with the sequence generated from gray code generator. The patterns generated from the Exclusive-OR array are the final output patterns.

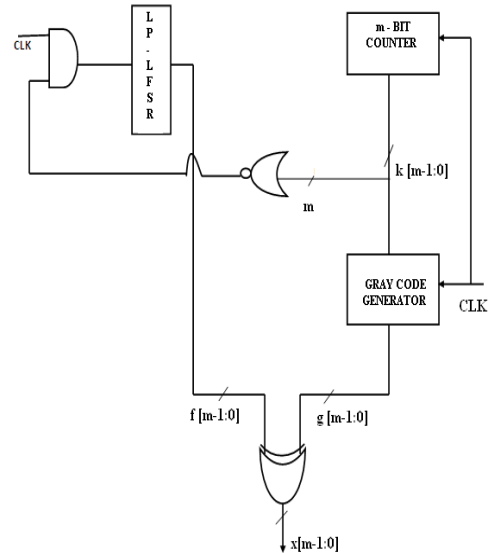


Fig.3 Low power test pattern generator

VI. LP-LFSR ALGORITHM

The LP-LFSR algorithm is given below:

- Consider a N-bit internal (or) external linear feedback shift register  $[n > 2]$ .
- For example n-bit, external LFSR is considered, which consists of n-flip flops in series. A common clock signal is applied for all flip flops as control signal.
- For exchanging the output of adjacent flip flops, multiplexers are used. The output of the last stage flip flop is taken as a select line.
- If the output of last stage flip flop is Zero, swapping will not be carried out.
- If the output of last stage flip flop is one, any one of the flip flop output is swapped with its adjacent flip flop output value.
- From other flip flops, the output will be taken as such.
- If the LFSR is moved through a complete cycle of  $2^n$  states then expected transitions are  $2^{n-1}$ . When the output of the adjacent flip flops are swapped, the expected transitions are  $2^{n-2}$ . Thus, the transitions produced are reduced by 50% compared with original LFSR. The transition reduction is concentrated mainly on any one of the multiplexer output.
- Gray converter modifies the counter output such that two successive values of its output are differing in only one bit. Gray converters can be implemented as shown in next page.

$$\begin{aligned}
 g[n-1] &= k[n-1] \\
 g[n-2] &= k[n-1] \text{ XOR } k[n-2] \\
 &\vdots \\
 &\vdots \\
 &\vdots \\
 g[2] &= k[2] \text{ XOR } k[3] \\
 g[1] &= k[1] \text{ XOR } k[2] \\
 g[0] &= k[0] \text{ XOR } k[1]
 \end{aligned}$$

S.C.Lei et al.,[13] proposed that the conventional LFSR’s output seeds cannot be taken directly, because some seeds may share the same vectors. Thus the LP-LFSR should ensure that any two of the single input changing sequences don’t share the same vectors or share as few vectors as possible. Test patterns generated from the proposed structure are implemented as following equations.

$$\begin{aligned}
 x[0] &= f[0] \text{ XOR } g[0] \\
 x[1] &= f[1] \text{ XOR } g[1] \\
 x[2] &= f[2] \text{ XOR } g[2] \\
 x[3] &= f[3] \text{ XOR } g[3] \\
 x[4] &= f[4] \text{ XOR } g[4] \\
 x[5] &= f[5] \text{ XOR } g[5] \\
 &\vdots \\
 &\vdots \\
 &\vdots \\
 X[n-1] &= f[n-1] \text{ XOR } g[n-1]
 \end{aligned}$$

Thus, the XOR result of the sequences is single input changing sequence. In turn reduces the switching activity and hence, the power dissipation is very less compared with conventional LFSR. The below patterns shows the counter and its respective gray value. It is shown that all values of g[2:0] are single input changing patterns.

Patterns:

K [2:0]	g [2:0]
K0= 000	g0= 000
K1= 001	g1= 001
K2= 010	g2= 011
K3= 011	g3= 010
K4= 100	g4= 110
K5= 101	g5= 111
K6= 110	g6= 101
K7= 111	g7= 100

## VII. IMPLIMENTATION DETAILS

To validate the effectiveness of the proposed method, we select test pattern generator (TPG) using conventional linear feedback shift register [LFSR] for comparison with proposed system. Table 1 shows the power consumption comparison between TPG using conventional LFSR and the proposed LP-LFSR after applying the generated patterns to the 4x4 braun array multiplier.

The static power dissipation from conventional LFSR and proposed LP-LFSR are shown.

TABLE-1  
COMPARISION OF POWER DISSIPATION

	Conventional LFSR with 4x4	Proposed LP-LFSR with 4x4
<b>Registers</b>	81	--
<b>Frequency (MHz)</b>	132.33	107.7
<b>Static power dissipation (mW)</b>	80.03	59.84

From the implementation details, it is verified that the presented method gives better power reduction compared to the existing method.

## VIII. CONCLUSION

A low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR). The sequence generated from LP-LFSR is Ex-ORed with the single input changing sequences generated from gray code generator, which effectively reduces the switching activities between the test patterns. Thus, the proposed method reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR instead of conventional LFSR.

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